What is claimed is:

1. A method of making a low-pin-count chip package comprising the steps of:

providing a metal carrier plate having opposing upper and lower surfaces, the upper surface of the metal carrier plate having a central bulge for receiving a semiconductor chip and a plurality of peripheral bulge arranged at the periphery of the central bulge, the upper surfaces of the central bulge and the peripheral bulges having a first metal coating formed thereon, the lower surface of the metal carrier plate having a second metal coating formed corresponding to the first metal coating;

attaching a semiconductor chip onto the central bulge of the metal carrier plate;

electrically coupling the semiconductor chip to the peripheral bulges of the metal carrier plate;

forming a package body over the semiconductor chip and the metal carrier plate; and

etching areas on the lower surface of the metal carrier plate without protection of the second metal coating such that the central bulge and each of the peripheral bulges are separated from one another so as to form a die pad and a plurality of connection pads.

2. The method as claimed in claim 1, wherein the metal carrier plate is formed from the steps of:

providing a copper foil having opposing upper and lower surfaces;

applying a first photoresist layer on the upper surface of the copper foil and a second photoresist layer on the lower surface of the copper foil;

photoimaging and developing the photoresist layers so as to expose predetermined portions of the copper foil;

forming the first metal coating on the exposed portions of the upper surface of the copper foil and the second metal coating on the exposed portions of the lower surface of the copper foil;

stripping the first photoresist layer;

half-etching areas on the upper surface of the copper foil exposed from the first metal coating so as to form the central bulge and the peripheral bulges; and

stripping the second photoresist layer.

3. The method as claimed in claim 1, wherein each of the first and the second metal coating comprises a layer of nickel covering the surface of the copper foil, and a layer of metal selected from the group consisted of gold and palladium covering the nickel layer.

4. A low-pin-count chip package comprising:

a die pad and a plurality of connection pads arranged at the periphery of the die pad wherein the die pad and the connection pads have a concave profile;

a first metal coating on the upper surface of the die pad and the connection pads;

a semiconductor chip disposed on the die pad and electrically coupled to the connection pads;

a package body formed over the semiconductor chip and the connection pads in a manner that a portion of the die pad and a portion of each connection pad extend outward from the bottom of the package body; and

a second metal coating on the lower surface of the die pad and the connection pads.

5. The low-pin-count chip package as claimed in claim 4, wherein each of the first and the second metal coating comprises a layer of nickel covering the surface of the die pad and the connection pads, and a layer of metal selected from the group consisted of gold and palladium covering the nickel layer.

6. The low-pin-count chip package as claimed in claim 4, wherein the extension portions of the die pad and each connection pad have a height of at least 2 mils.

7. The low-pin-count chip package as claimed in claim 4, wherein areas on the surfaces of the die pad and each connection pad without protection of the package body have a third metal coating formed thereon thereby avoiding corrosion and contamination.

8. A method of making a low-pin-count chip package comprising the steps of:

providing a metal carrier plate having opposing upper and lower surfaces, the upper surface of the metal carrier plate having a die receiving area and a plurality of peripheral bulge arranged at the periphery of the die receiving area, the upper surfaces of the peripheral bulges having a first metal coating formed thereon, the lower surface of the metal carrier plate having a second metal coating formed corresponding to the first metal coating;

attaching a semiconductor chip onto the die receiving area of the metal carrier plate;

electrically coupling the semiconductor chip to the peripheral bulges of the metal carrier plate;

forming a package body over the semiconductor chip and the metal carrier plate; and

etching areas on the lower surface of the metal carrier plate without protection of the second metal coating such that each of the peripheral bulges is separated from one another so as to form a plurality of connection pads.

9. The method as claimed in claim 8, wherein the metal carrier plate is formed from the steps of:

providing a copper foil having opposing upper and lower surfaces;

applying a first photoresist layer on the upper surface of the copper foil and a second photoresist layer on the lower surface of the copper foil;

photoimaging and developing the photoresist layers so as to expose predetermined portions of the copper foil;

forming the first metal coating on the exposed portions of the upper surface of the copper foil and the second metal coating on the exposed portions of the lower surface of the copper foil;

stripping the first photoresist layer;

half-etching areas on the upper surface of the copper foil exposed from the first metal coating so as to form the peripheral bulges; and

stripping the second photoresist layer.

10. The method as claimed in claim 8, wherein each of the first and the second metal coating comprises a layer of nickel covering the surface of the copper foil, and a layer of metal selected from the group consisted of gold and palladium covering the nickel layer.

11. A low-pin-count chip package comprising:

a semiconductor chip;

a plurality of connection pads arranged at the periphery of the semiconductor chip wherein the connection pads have a concave profile;

a first metal coating on the upper surface of the connection pads;

the semiconductor chip having a plurality of bonding pads electrically coupled to the connection pads;

a package body formed over the semiconductor chip and the connection pads in a manner that a portion of each connection pad extends outward from the bottom of the package body; and

a second metal coating on the lower surface of the connection pads.

12. The low-pin-count chip package as claimed in claim 11, wherein each of the first and the second metal coating comprises a layer of nickel covering the surface of the connection pads, and a layer of metal selected from the group consisted of gold and palladium covering the nickel layer.

13. The low-pin-count chip package as claimed in claim 11, wherein the extension portion of each connection pad has a height of at least 2 mils.

14. The low-pin-count chip package as claimed in claim 11, wherein areas on the surface of each connection pad without protection of the package body have a third metal coating formed thereon thereby avoiding corrosion and contamination.